AMENDMENTS TO THE CLAIMS:

Kindly amend claims 1-7, and add new claims 8-13 as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter [[for]] performing half-band processing to a sample output of said ~~a sampling output of a~~ digital signal, ~~outputted by said A/D converter~~ and [[for]] attenuating a frequency component other than a predetermined normal ~~band from a frequency component~~ frequency band included in the ~~sampling~~ sample output; and

an anti-aliasing circuit for suppressing or removing ~~noise having an aliasing band, which is~~ aliasing noise having an aliasing frequency band caused by the half-band processing in said digital filter, [[by]] said noise is suppressed or removed using a sign signal output[[ted]] from said digital filter.

Claim 2 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit determines whether the output from said digital filter~~, which is subjected to said half-band processing,~~ is a pass signal with the having the normal frequency band or a pass signal having the aliasing ~~signal~~ frequency band, ~~based on~~ using a changing period of the sign signal output[[ted]] from said digital filter, [[and]] said anti-aliasing circuit suppresses or removes only the pass signal having the aliasing frequency band.

Claim 3 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit comprises: (limitations of claim 3 is added to claim 1)

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a period measuring circuit for ~~measuring a changing~~ generating measurement of period changes in [[of]] the sign signal output[[ted]] by said digital filter;

a threshold holding circuit for ~~holding~~ setting a threshold equal to a period of an intermediate frequency between the normal frequency band and the aliasing frequency band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold, ~~which is set to said threshold holding circuit~~ and for outputting a shift control signal when it is determined that the measurement of ~~period measured by~~ said period measuring circuit is not larger than the threshold; and

a shift register for shifting a signal which is input[[ted]] from said digital filter and [[is]] stored, based on said shift control signal, and for suppressing an amplitude of the aliasing noise.

Claim ~~4~~ 3 (currently amended): The apparatus according to claim ~~3~~ 1, wherein said anti-aliasing circuit further comprises a shift value setting register, to which the number of shift bits is set when the signal, ~~which is inputted from said digital filter and is stored,~~ is subjected to shift processing by said shift register.

Claim ~~5~~ 4 (currently amended): The apparatus according to claim ~~3~~ 1, wherein said anti-aliasing circuit further comprises a delay circuit for delaying the output from said digital filter by a delay time which ~~is taken by the measurement by said period measuring circuit and the comparison calculation by said comparator~~ corresponds to a time for said comparator to output said shift control signal.

Claim ~~6~~ 5 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit comprises:

a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter;

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a threshold holding circuit for holding a period of an intermediate frequency between the normal frequency band and the aliasing frequency band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set [[to]] by said threshold holding circuit and [[for]] outputting a clear signal when it is determined that the period is not larger than the threshold set by said threshold holding circuit; and

a delay circuit for delaying the output from said digital filter by a delay time which ~~is taken by the measurement of said period measuring circuit and the comparison calculation of said comparator~~ corresponds to a time for said comparator to output said shift control signal and for erasing a signal during delay processing when said clear signal is inputted.

Claim 6 (currently amended): A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter [[for]] performing half-band processing to a sample output of said ~~a sampling output of a~~ digital signal, ~~outputted by said A/D converter~~ and [[for]] attenuating a frequency component other than a predetermined normal ~~band from a frequency component~~ frequency band included in the sample ~~sampling~~ output;

an edge-detection circuit for detecting an edge of a sign signal ~~which is~~ output[[ted]] by said digital filter and for generating a set pulse;

a period measuring circuit for ~~measuring a changing~~ generating a measurement of period changes in [[of]] the sign signal which is output[[ted]] by said digital filter;

a threshold holding circuit for ~~holding~~ setting a threshold equal to a period of an intermediate frequency between a normal frequency band and an aliasing frequency band;

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a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold ~~held by said threshold holding circuit~~ and for outputting a reset pulse when ~~it is determined that~~ the period is not larger than the threshold; and

a detection register outputting a first signal when ~~for inputting~~ said set pulse is received as input thereby placing said detection register ~~so as to be~~ in a set state and ~~outputting a first level and for inputting~~ outputting a second signal when said reset pulse is input thereby placing said detector register ~~so as to be~~ in said reset state ~~and outputting a second level~~.

Claim ~~8~~ 7 (new). A digital signal processing apparatus comprising:

a digital filter performing half-band processing on a digital signal to output a processed signal and a sign signal; and

an anti-aliasing circuit coupled to said digital filter to suppress or remove an aliasing noise from said processed signal by use of said sign signal.

Claim ~~9~~ 8 (new). The apparatus according to Claim ~~8~~ 7, wherein said anti-aliasing circuit determines whether the output from said digital filter, which is subjected to said half-band processing, is a pass signal having a normal band or a pass signal having the aliasing signal, based on a changing period of the sign signal outputted from said digital filter, and suppresses or removes only the pass signal having the aliasing band.

Claim 10 (new). The apparatus according to claim 8, wherein said anti-aliasing circuit comprises: a period measuring circuit for measuring a changing period of the sign signal outputted by said digital filter; a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band; a comparator for comparing and determining whether or not the period measured by said period measuring

(limitations of claim 10 is added to claim 8)
(which is renumbered as claim 7)

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circuit is larger than the threshold which is set to said threshold holding circuit and for outputting a shift control signal when it is determined that the period measured by said period measuring circuit is not larger than the threshold; and a shift register for shifting a signal which is inputted from said digital filter and is stored, based on said shift control signal, and for suppressing an amplitude of the aliasing noise.

Claim ~~11~~ 9 (new). The apparatus according to claim ~~10~~ 7, wherein said anti-aliasing circuit further comprises a shift value setting register, to which the number of shift bits is set when the signal, which is inputted from said digital filter and is stored, is subjected to shift processing by said shift register.

Claim ~~12~~ 10 (new). The apparatus according to claim ~~10~~ 7, wherein said anti-aliasing circuit further comprises a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement by said period measuring circuit and the comparison calculation by said comparator.

Claim ~~13~~ 11 (new). The apparatus according to claim ~~8~~ 7, wherein said anti-aliasing circuit comprises: a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter; a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band; a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set to said threshold holding circuit and for outputting a clear signal when it is determined that the period is not larger than the threshold; and a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement of said period measuring circuit and the comparison calculation of said comparator and for erasing a signal during delay processing when said clear signal is inputted.

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AMENDMENTS TO THE CLAIMS:

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This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter [[for]] performing half-band processing to a sample output of said ~~a sampling output of a~~ digital signal, ~~outputted by said A/D converter~~ and [[for]] attenuating a frequency component other than a predetermined normal ~~band from a frequency component~~ frequency band included in the ~~sampling~~ sample output; and

an anti-aliasing circuit for suppressing or removing ~~noise having an aliasing band, which is~~ aliasing noise having an aliasing frequency band caused by the half-band processing in said digital filter, [[by]] said noise is suppressed or removed using a sign signal output[[ted]] from said digital filter.

Claim 2 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit determines whether the output from said digital filter~~, which is subjected to said half-band processing,~~ is a pass signal with the having the normal frequency band or a pass signal having the aliasing ~~signal~~ frequency band, ~~based on~~ using a changing period of the sign signal output[[ted]] from said digital filter, [[and]] said anti-aliasing circuit suppresses or removes only the pass signal having the aliasing frequency band.

Claim 3 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit comprises:

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a period measuring circuit for ~~measuring a changing~~ generating measurement of period changes in [[of]] the sign signal output[[ted]] by said digital filter;

a threshold holding circuit for ~~holding~~ setting a threshold equal to a period of an intermediate frequency between the normal frequency band and the aliasing frequency band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold, ~~which is set to said threshold holding circuit~~ and for outputting a shift control signal when it is determined that the measurement of ~~period measured by~~ said period measuring circuit is not larger than the threshold; and

a shift register for shifting a signal which is input[[ted]] from said digital filter and [[is]] stored, based on said shift control signal, and for suppressing an amplitude of the aliasing noise.

Claim 4 (currently amended): The apparatus according to claim 3, wherein said anti-aliasing circuit further comprises a shift value setting register, to which the number of shift bits is set when the signal~~, which is inputted from said digital filter and is stored,~~ is subjected to shift processing by said shift register.

Claim 5 (currently amended): The apparatus according to claim 3, wherein said anti-aliasing circuit further comprises a delay circuit for delaying the output from said digital filter by a delay time which ~~is taken by the measurement by said period measuring circuit and the comparison calculation by said comparator~~ corresponds to a time for said comparator to output said shift control signal.

Claim 6 (currently amended): The apparatus according to claim 1, wherein said anti-aliasing circuit comprises:

a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter;

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a threshold holding circuit for holding a period of an intermediate frequency between the normal frequency band and the aliasing frequency band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set [[to]] by said threshold holding circuit and [[for]] outputting a clear signal when it is determined that the period is not larger than the threshold set by said threshold holding circuit; and

a delay circuit for delaying the output from said digital filter by a delay time which ~~is taken by the measurement of said period measuring circuit and the comparison calculation of said comparator~~ corresponds to a time for said comparator to output said shift control signal and for erasing a signal during delay processing when said clear signal is inputted.

Claim 7 (currently amended): A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter [[for]] performing half-band processing to a sample output of said ~~a sampling output of a~~ digital signal, ~~outputted by said A/D converter~~ and [[for]] attenuating a frequency component other than a predetermined normal ~~band from a frequency component~~ frequency band included in the sample ~~sampling~~ output;

an edge-detection circuit for detecting an edge of a sign signal ~~which is~~ output[[ted]] by said digital filter and for generating a set pulse;

a period measuring circuit for ~~measuring a changing~~ generating a measurement of period changes in [[of]] the sign signal which is output[[ted]] by said digital filter;

a threshold holding circuit for ~~holding~~ setting a threshold equal to a period of an intermediate frequency between a normal frequency band and an aliasing frequency band;

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a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold ~~held by said threshold holding circuit~~ and for outputting a reset pulse when ~~it is determined that~~ the period is not larger than the threshold; and

a detection register outputting a first signal when ~~for inputting~~ said set pulse is received as input thereby placing said detection register ~~so as to be~~ in a set state and ~~outputting a first level and for inputting~~ outputting a second signal when said reset pulse is input thereby placing said detector register ~~so as to be~~ in said reset state ~~and outputting a second level~~.

Claim 8 (new). A digital signal processing apparatus comprising:

a digital filter performing half-band processing on a digital signal to output a processed signal and a sign signal; and

an anti-aliasing circuit coupled to said digital filter to suppress or remove an aliasing noise from said processed signal by use of said sign signal.

Claim 9 (new). The apparatus according to Claim 8, wherein said anti-aliasing circuit determines whether the output from said digital filter, which is subjected to said half-band processing, is a pass signal having a normal band or a pass signal having the aliasing signal, based on a changing period of the sign signal outputted from said digital filter, and suppresses or removes only the pass signal having the aliasing band.

Claim 10 (new). The apparatus according to claim 8, wherein said anti-aliasing circuit comprises: a period measuring circuit for measuring a changing period of the sign signal outputted by said digital filter; a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band; a comparator for comparing and determining whether or not the period measured by said period measuring

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circuit is larger than the threshold which is set to said threshold holding circuit and for outputting a shift control signal when it is determined that the period measured by said period measuring circuit is not larger than the threshold; and a shift register for shifting a signal which is inputted from said digital filter and is stored, based on said shift control signal, and for suppressing an amplitude of the aliasing noise.

Claim 11 (new). The apparatus according to claim 10, wherein said anti-aliasing circuit further comprises a shift value setting register, to which the number of shift bits is set when the signal, which is inputted from said digital filter and is stored, is subjected to shift processing by said shift register.

Claim 12 (new). The apparatus according to claim 10, wherein said anti-aliasing circuit further comprises a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement by said period measuring circuit and the comparison calculation by said comparator.

Claim 13 (new). The apparatus according to claim 8, wherein said anti-aliasing circuit comprises: a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter; a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band; a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set to said threshold holding circuit and for outputting a clear signal when it is determined that the period is not larger than the threshold; and a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement of said period measuring circuit and the comparison calculation of said comparator and for erasing a signal during delay processing when said clear signal is inputted.

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